19-2236; Rev 0; 10/01

MAXIM

Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

General Description

The MAX9380 is a high-speed, low-jitter 2:1 multiplexer for clock and data distribution applications. The device selects one of the two single-ended inputs and converts it to a differential output.

The MAX9380 features low part-to-part skew of 33ps and propagation delay of 263ps.

The MAX9380 operates from a +3.0V to +3.8V supply for LVPECL applications or from a -3.0V to -3.8V supply for LVECL applications. The input is selected by a single select input. The select and data inputs feature internal pulldown resistors that ensure a low default state if left open.

These devices are specified for operation from -40°C to +85°C, and are available in space-saving 8-pin µMAX and SO packages.

Features

- **>300mV Differential Output at 3.5GHz**
- **Low 20mA Supply Current**
- **33ps (typ) Part-to-Part Skew**
- **263ps (typ) Propagation Delay**
- **<0.2ps$_{RMS}$ Added Random Jitter**
- **High-Speed Select Input**
- **Output Low with Open Inputs**
- **Pin Compatible with MC10EP58**

Applications

Precision Clock Distribution

DSLAM

DLC

Base Station

ATE

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9380EUA*	-40°C to +85°C	8 µMAX
MAX9380ESA	-40°C to +85°C	8 SO-EP**

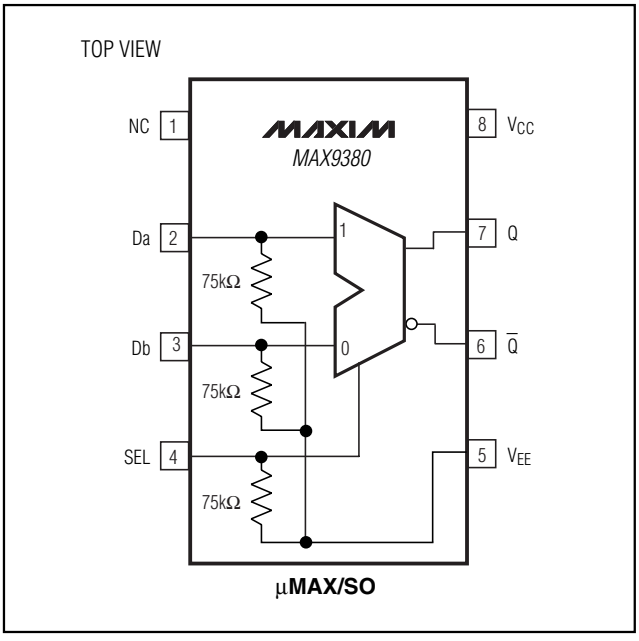
**Future product—contact factory for availability.*

***EP = Exposed paddle.*

Input/Output Function Table

INPUTS	OUTPUTS	
Da (SEL = high) or **Db (SEL =** low)	**Q**	$\overline{\mathbf{Q}}$
High	H	L
Low or open	L	H

Pin Configuration



Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} ..... -0.3V to +4.1V
Inputs (Da, Db, SEL) ..... V_{EE} - 0.3V to V_{CC} + 0.3V
Output Current (Continuous) 50mA
Output Current (Surge) 100mA
Junction-to-Ambient Thermal Resistance in Still Air
8-Pin µMAX ..... +221°C/W
8-Pin SO* ..... +170°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM Airflow
8-Pin µMAX ..... +155°C/W
8-Pin SO* ..... +99°C/W
Junction-to-Case Thermal Resistance
8-Pin µMAX ..... +39°C/W
8-Pin SO ..... +40°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
ESD Protection
Human Body Model (Inputs and Outputs) 2kV
Soldering Temperature (10s) ..... +300°C
* *Rating is for exposed paddle not connected.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +3.0V to +3.8V, outputs terminated with 50Ω to V_{CC} - 2.0V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUTS (Da, Db, SEL)												
Input High Voltage	V_{IH}		V_{CC} - 1.210		V_{CC} - 0.885	V_{CC} - 1.145		V_{CC} - 0.820	V_{CC} - 1.085		V_{CC} - 0.760	V
Input Low Voltage	V_{IL}		V_{CC} - 1.935		V_{CC} - 1.610	V_{CC} - 1.870		V_{CC} - 1.545	V_{CC} - 1.81		V_{CC} - 1.485	V
Input High Current	I_{IH}	V_{IN} = $V_{IH(MAX)}$			150			150			150	µA
Input Low Current	I_{IL}	V_{IN} = $V_{IL(MIN)}$	0.5			0.5			0.5			µA
OUTPUTS (Q, $\overline{Q}$)												
Single-Ended Output High Voltage	V_{OH}	Figure 1	V_{CC} - 1.135	V_{CC} - 0.979	V_{CC} - 0.885	V_{CC} - 1.07	V_{CC} - 0.959	V_{CC} - 0.82	V_{CC} - 1.01	V_{CC} - 0.947	V_{CC} - 0.76	V
Single-Ended Output Low Voltage	V_{OL}	Figure 1	V_{CC} - 1.935	V_{CC} - 1.721	V_{CC} - 1.685	V_{CC} - 1.87	V_{CC} - 1.698	V_{CC} - 1.62	V_{CC} - 1.81	V_{CC} - 1.681	V_{CC} - 1.56	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1	550	748		550	741		550	734		mV
POWER SUPPLY												
Supply Current	I_{EE}	(Note 4)		18	26		20	26		22	30	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +3.0V to +3.8V, outputs loaded with 50Ω to V_{CC} - 2V, V_{IH} = V_{CC} - 1.11V, V_{IL} = V_{CC} - 1.53V, input frequency = 2.0GHz, input transition time = 125ps (20% to 80%). Typical values are at V_{CC} - V_{EE} = +3.3V, unless otherwise noted.) (Notes 1, 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Data Input-to-Output Delay	t_{PLH1}, t_{PHL1}	Figure 1	176	258	298	192	263	316	222	277	385	ps
Select Input-to-Output Delay	t_{PLH2}, t_{PHL2},	Figure 2	210	304	329	219	308	360	247	318	392	ps
Part-to-Part Skew	t_{SKPP}	Data input to output (Note 6)		27	122		33	124		14	163	ps
Added Random Jitter (Note 7)	t_{RJ}	f_{IN} = 3.2GHz, clock pattern			1.2		0.2	1.2			1.2	ps (RMS)
Added Deterministic Jitter (Note 7)	t_{DJ}	2.0Gbps, 2^{23} - 1 PRBS			51		36	51			51	ps (p-p)
		3.2Gbps, 2^{23} - 1 PRBS			77		48	77			77	
Switching Frequency	f_{MAX}	Figure 1, V_{OH} - V_{OL} ≥ 300mV	3.0	3.5		3.0	3.5		3.0	3.5		GHz
		Figure 1, V_{OH} - V_{OL} ≥ 550mV	2.0			2.0			2.0			
Output Rise/Fall Time (20% to 80%)	t_R, t_F	Figure 1	50		96	50		96	50		98	ps

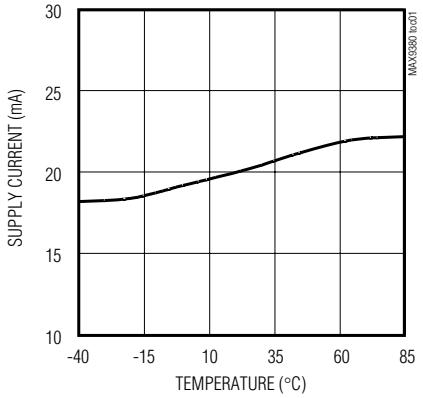
Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterization over the full operating temperature range.
Note 4: All pins are open except V_{CC} and V_{EE}.
Note 5: Guaranteed by design and characterization. Limits are set to ±6 sigma.
Note 6: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 7: Device jitter added to the input signal.

Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

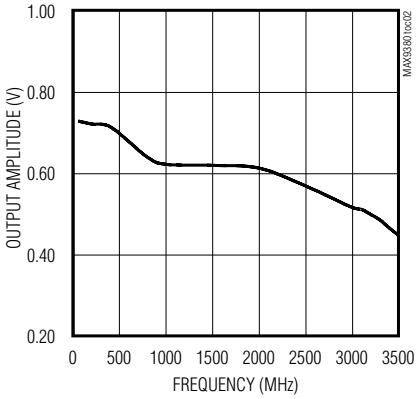
Typical Operating Characteristics

(V_{CC} - V_{EE} = +3.3V, V_{IH} = V_{CC} - 1.165V, V_{IL} = V_{CC} - 1.475V, outputs loaded with 50Ω to V_{CC} - 2.0V, input frequency = 1GHz, input transition time = 125ps (20% to 80%), unless otherwise noted.)

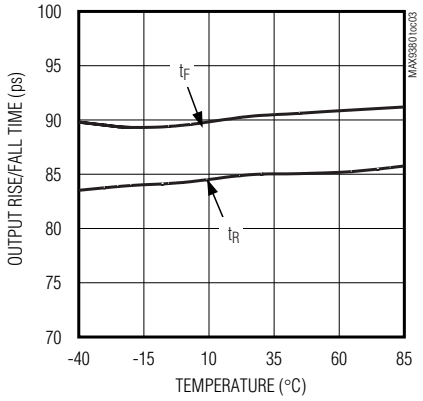
SUPPLY CURRENT (I_{EE}) vs. TEMPERATURE



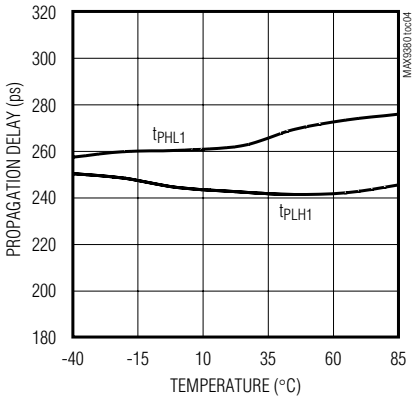
OUTPUT AMPLITUDE (V_{OH} - V_{OL}) vs. FREQUENCY



OUTPUT RISE/FALL TIME vs. TEMPERATURE



PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	NC	No Connection. Not internally connected.
2	Da	Single-Ended LVECL/LVPECL Data Input. Da is low default through internal 75kΩ pulldown resistor.
3	Db	Single-Ended LVECL/LVPECL Data Input. Db is low default through internal 75kΩ pulldown resistor.
4	SEL	Single-Ended Control Input. SEL is low default through an internal 75kΩ pulldown resistor selecting Db. Setting SEL to high selects Da.
5	V_{EE}	Negative Supply Voltage
6	$\overline{Q}$	Differential LVECL/LVPECL Output. Open Emitter. $\overline{Q}$ is default high when inputs are open.
7	Q	Differential LVECL/LVPECL Output. Open Emitter. Q is default low when inputs are open.
8	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to V_{EE} with 0.1µF and 0.01µF capacitors as close to the device as possible, with the smaller capacitor closest to the IC.
Exposed Paddle	EP	Exposed paddle (MAX9380ESA-EP only). Connect to V_{EE} internally. See package dimension.

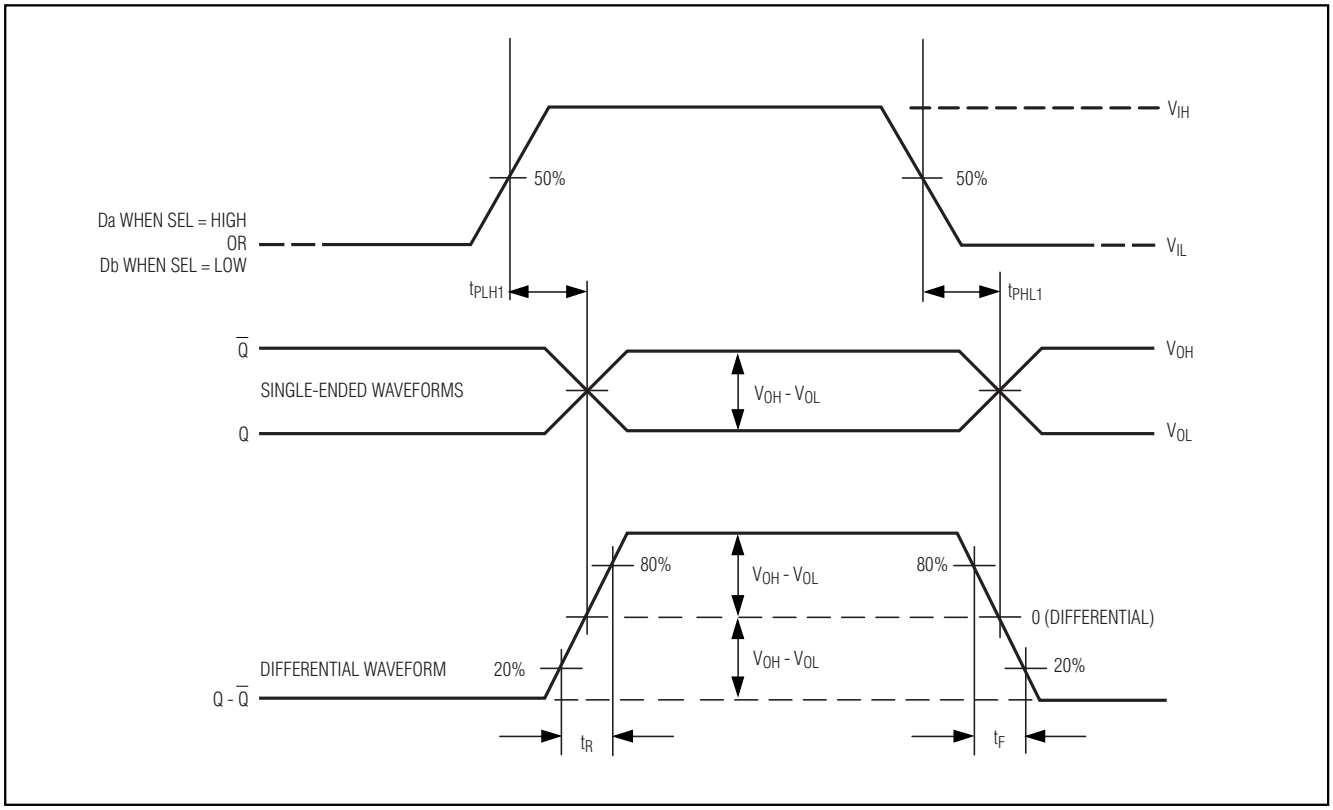


Figure 1. Data Input-to-Output Propagation Delay and Transition Timing Diagram

Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

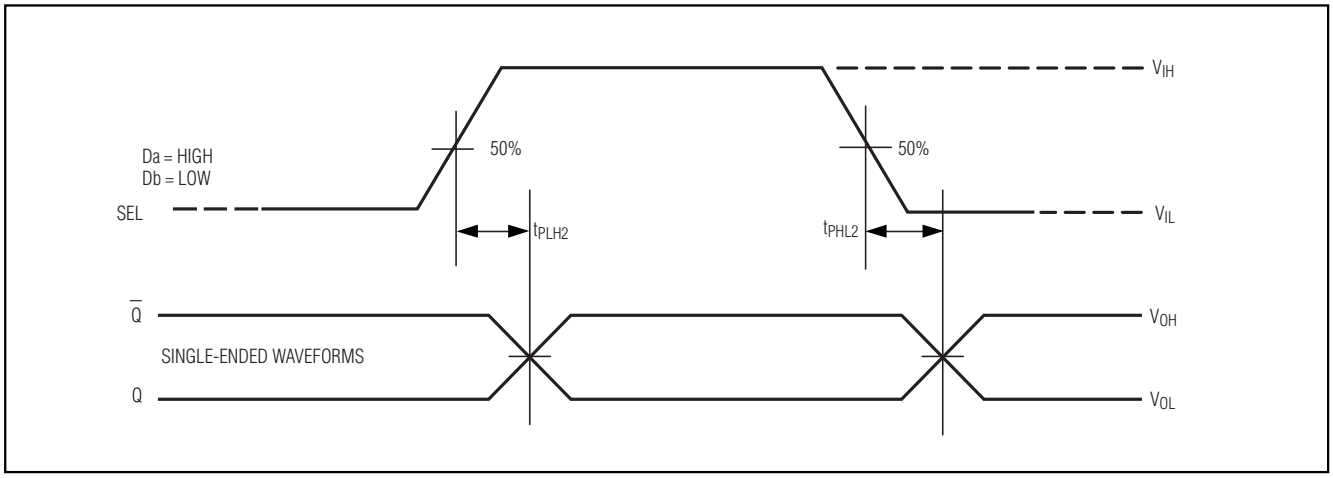


Figure 2. Select Input-to-Output Propagation Delay and Transition Timing Diagram

Detailed Description

The MAX9380 is a high-speed, low-jitter 2:1 multiplexer designed for clock and data distribution. The device selects one of the two single-ended inputs.

The multiplexer function is controlled by the single-ended SEL input. A high level on the SEL input selects the single-ended data input Da. Similarly, a low level on the SEL input selects the single-ended data input Db. The selected input is converted to a differential signal at the Q and $\overline{Q}$ outputs.

The inputs Da, Db, and SEL have a 75kΩ pulldown to V_{EE}. This ensures that an open input has a low state. All inputs can be driven from a single-ended LVECL/LVPECL signal or to V_{EE} and V_{CC}.

Applications Information

LVECL/LVPECL

In LVECL systems, the positive supply voltage is conventionally chosen to be system ground. This arrangement produces the best noise immunity since ground is normally a system-wide reference voltage. Operate the MAX9380 with V_{CC} = 0 (ground) and V_{EE} = -3.3V for an LVECL system.

The MAX9380 operates in LVPECL systems by connecting V_{EE} to ground and V_{CC} to a positive supply voltage. Connect V_{CC} = +3.3V and V_{EE} = 0 for an LVPECL system.

Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize the performance and noise immunity. This is particularly true of use in an LVPECL system where the power-supply voltage is used as a reference. Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF capacitor closest to the device pins. Use multiple parallel vias for ground plane connection to minimize inductance.

Circuit Board Traces

Input and output trace characteristics affect the performance of ECL devices. Connect each of the MAX9380 inputs and outputs to a 50Ω characteristic impedance trace. Avoid discontinuities in differential impedance and maximize common-mode noise immunity by maintaining the distance between differential traces and avoid sharp corners. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Output Termination

Terminate outputs through 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if the Q output of the MAX9380 is connected to a single-ended input, terminate both the Q and $\overline{Q}$ outputs.

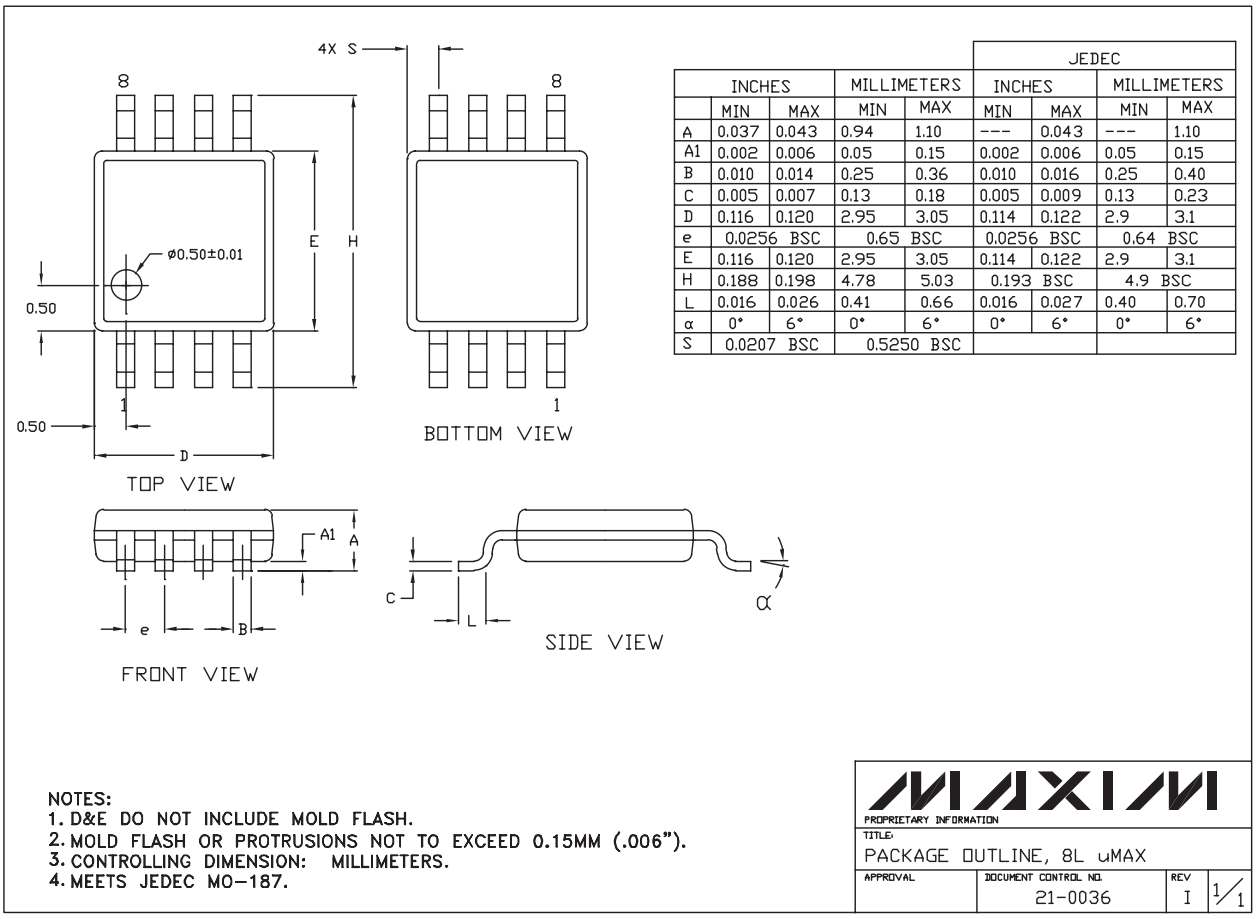
Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

Chip Information

TRANSISTOR COUNT: 242

PROCESS: Bipolar

Package Information



	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC					

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.

MAXIM
PROPRIETARY INFORMATION

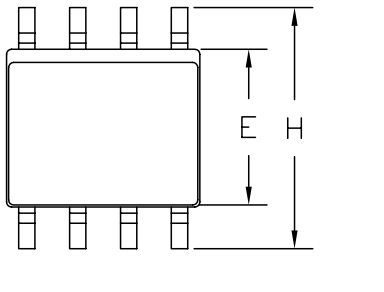
TITLE: PACKAGE OUTLINE, 8L uMAX

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0036	I	1/1

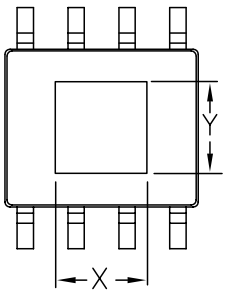
Single-Ended-to-Differential LVECL/LVPECL 2:1 Multiplexer

Package Information (continued)

8L, SOIC EXP. PAD.EPS

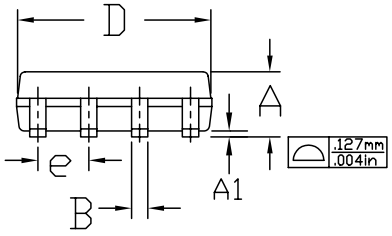


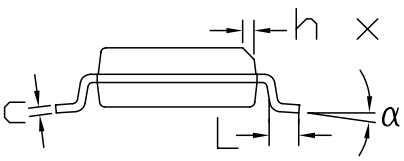
TOP VIEW



BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°
X	.082	.098	2.08	2.49
Y	.082	.098	2.08	2.49





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AA.
5. DIMENSIONS X AND Y DEFINE EXPOSED PAD METAL AREA.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE 8L SOIC, .150" EXPOSED PAD

APPROVAL	DWG	REV	
	21-0111	A	1/1